

The AD7574 Analog to Microprocessor Interface

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INTRODUCTION

The AD7574 is a low cost 8-bit ADC designed for easy interface to microprocessors as a memory mapped input device.

It uses a successive-approximations conversion technique, runs with an internal or external clock and can complete an 8-bit A/D conversion in 15 microseconds.

The analog to digital conversion operations are controlled by two logic inputs labelled $\overline{CS}$ (Chip Select) and $\overline{RD}$ ($\overline{READ}$). Conversion-in-progress indication is provided by a $\overline{BUSY}$ output signal (see Figure 1).

This note is intended to describe the AD7574 in its three main microprocessor interface modes with references to external clock source, input range switching and input multiplexing applications.

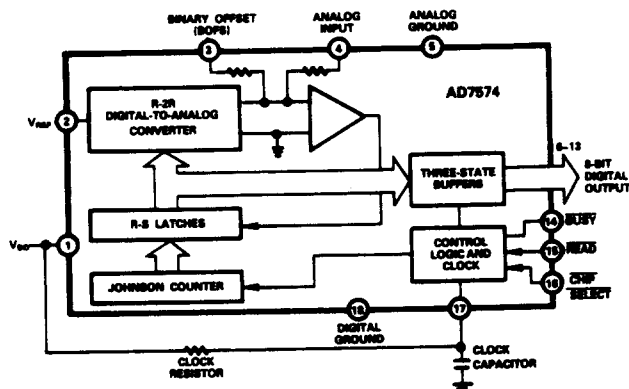


Figure 1. Inside the AD7574

INTERFACE MODES

Since the AD7574 is designed for use in memory mapped applications it can simulate RAM, ROM, or SLOW-ROM memories and can be controlled using standard chip select, READ and WRITE signals common to all memory systems.

ROM MODE

The ROM Mode is the easiest mode in which to use the AD7574. It appears in the processor memory map as one byte of Read Only Memory. One instruction from the CPU both reads conversion data and initiates a new conversion.

Basic Operation: The processor reads the 8 bits of data generated by a previous A/D conversion by executing a READ instruction from the memory address location assigned to the AD7574. When the processor $\overline{RD}$ signal goes LOW the AD7574 three state drivers are activated, placing the conversion data onto the processor data bus.

At the end of the READ instruction the AD7574 $\overline{RD}$ input is returned HIGH, resetting the device and initiating a new A/D conversion sequence (see Figure 2).

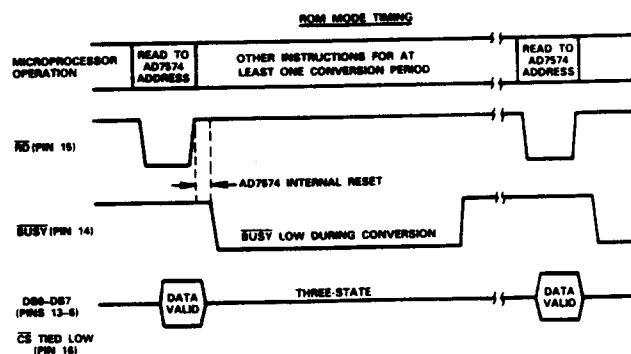


Figure 2.

Typical ROM MODE interface circuits for 8080 and 8085 microprocessors are shown in Figures 3 and 4. Most processors can be configured to operate with the AD7574 in this mode. Note: Any attempt to read data from the AD7574 during a conversion operation will result in incorrect data being read.

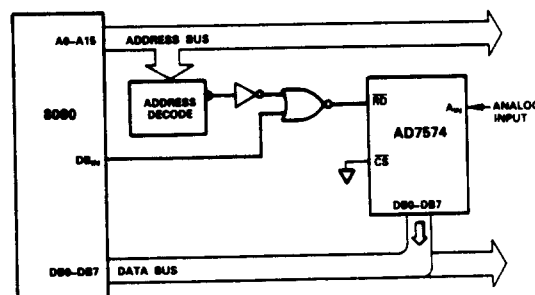


Figure 3. AD7574 to 8080 ROM-MODE Interface

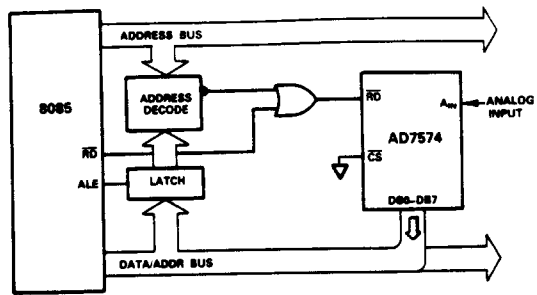


Figure 4. AD7574 to 8085 ROM-MODE Interface

Applications Of The Rom Mode

The advantage of this mode is its simplicity in both software and hardware terms. Reading conversion data is accomplished by just one memory READ instruction. However, it must be remembered that the data read will be the result of the previous conversion operation. This means that the time reference for the data sample will depend on when the previous READ operation finished. In applications where this uncertainty creates problems it can be eliminated by executing two READ operations separated by a software delay as shown in Figure 5.

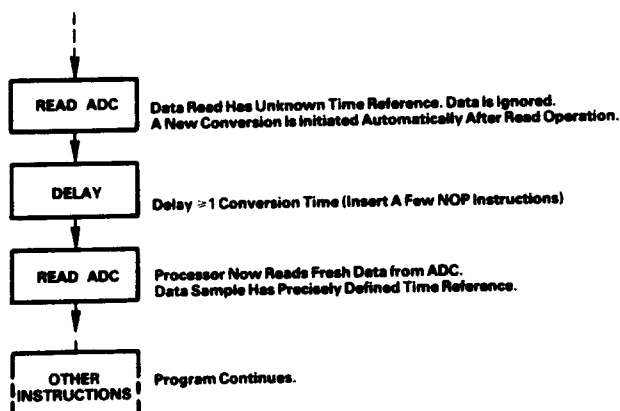


Figure 5. Defining the Data Sample Time Reference (ROM-MODE)

RAM MODE

Basic Operation

In the RAM MODE the AD7574 appears in the processor memory map as one byte of memory. A WRITE command initiates a conversion and a READ command reads the conversion data.

This mode offers complete control over the converter operation. The time reference for the data sample is defined by the WRITE command. The conversion data can be read any time after the conversion has finished.

In the RAM MODE a memory WRITE operation starts a conversion without modifying any of the microprocessor accumulators. (In the ROM mode, using a READ instruction to start a conversion means modifying an accumulator unnecessarily.) So, in situations where the age of a sample is important the RAM MODE makes for simpler, more logical software than the ROM MODE at the expense of requiring slightly more logic to drive $\overline{CS}$ and $\overline{RD}$ (see Figures 8 and 9).

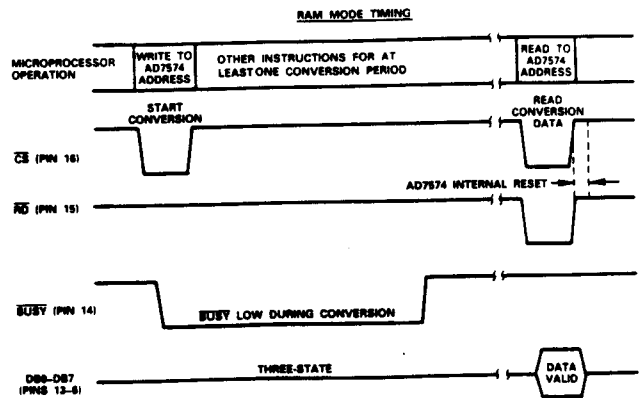


Figure 6.

Ram Mode Timing Considerations

1. $\overline{BUSY}$ must be high before a data read is attempted, i.e., delay from conversion start to data read must be at least as great as the AD7574 conversion time. In some situations it is possible to use the AD7574 $\overline{BUSY}$ output to halt the microprocessor for the duration of the conversion period thus simplifying the software requirements.
2. $\overline{CS}$ must return HIGH within 250ns after $\overline{RD}$ goes HIGH otherwise a new conversion may be initiated and the AD7574 will begin operating in the ROM mode (see Figure 7).

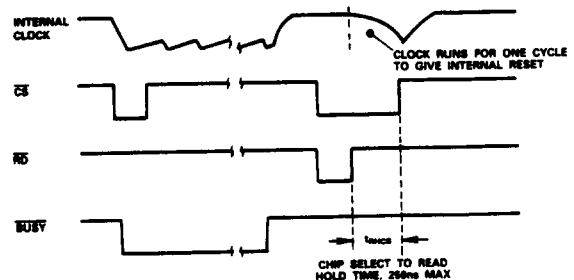


Figure 7. Chip Select to Read Timing

When $\overline{RD}$ returns high the AD7574 begins an internal reset cycle to prepare for the next conversion sequence. If $\overline{CS}$ has not returned high before the end of this reset operation, a conversion start will be detected and a new conversion initiated.

The duration of the internal reset cycle is dependent on the amount of capacitance on the clock pin (pin 17). The maximum value for t_{RHCS} guaranteed is 250ns at 25°C (see data sheet).

3. Conversion data may only be read from the AD7574 once, as after each read operation an internal reset is performed which destroys the data.
4. $\overline{CS}$ LOW has no effect while a conversion is in progress.
5. $\overline{RD}$ has no effect while $\overline{CS}$ is HIGH.

Typical RAM Mode interface circuits for the 8085 and 6800 are shown in Figures 8 and 9 respectively.

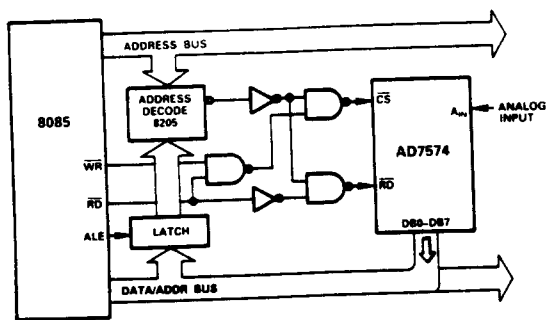


Figure 8. AD7574 to 8085 RAM Mode Interface

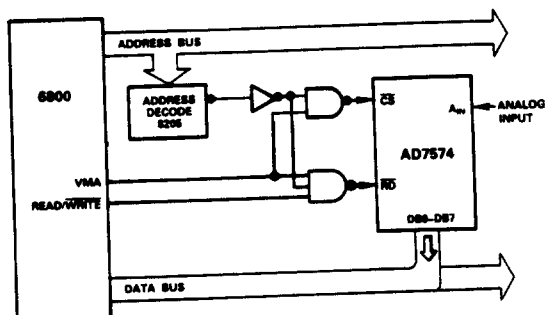


Figure 9. AD7574 to 6800 RAM Mode Interface

SLOW MEMORY MODE

This is by far the most elegant mode of operation for the AD7574. Every read instruction produces fresh data so that there is no doubt about the age of the sample.

Basic Operation

The slow memory mode is intended for use with processors which can be forced into a wait state for at least 15μs (such as the 8080, 8085 and SC/MP). It allows the processor to start a conversion, wait until the $\overline{\text{BUSY}}$ flag is HIGH and then read data, all during execution of a single memory read instruction (see Figure 10).

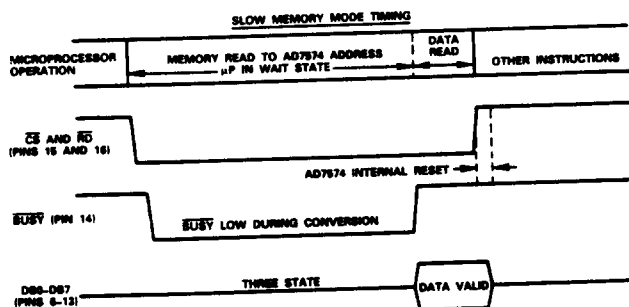


Figure 10.

Wait State

Many processors test the condition of the READY/WAIT input very soon after the start of an instruction cycle. For this reason the timing of the AD7574 and its associated address decode logic must be such that $\overline{\text{BUSY}}$ goes LOW early enough in the processor instruction cycle for the READY/WAIT input to be effective in forcing the processor into a WAIT State.

Bus Conflict

In applications where the processors memory READ/ WRITE signal is not available early enough in the machine

cycle for it to be used to enable or disable the address decode logic, the system software must be such that a WRITE operation to the AD7574 address is never attempted. If this precaution is not taken, Bus Conflicts will occur due to the AD7574 outputting data onto the data bus while the CPU is also driving the data bus.

Typical slow memory mode interface circuits for 8085 and SC/MP microprocessors are shown in Figures 11 and 12.

8085 Interface (Figure 11)

For simplicity, only the upper 8 address bits of the 8085 address bus are decoded to select the AD7574. Invalid address states are eliminated by using ALE to drive an address latch.

The processor SO status signal provides the earliest possible indication that a READ operation is about to occur, $\text{SO} = 0$ for a READ operation. Since, with the processor on a fast clock the READ signal could occur too late to enable the address decode logic, the SO signal is a convenient alternative, eliminating any possibility of a bus conflict during WRITE operations.

SC/MP Interface (Figure 12)

Similar to the 8085 application. Address decode is gated with negative READ strobe and $\overline{\text{BUSY}}$ drives the SC/MP negative hold input.

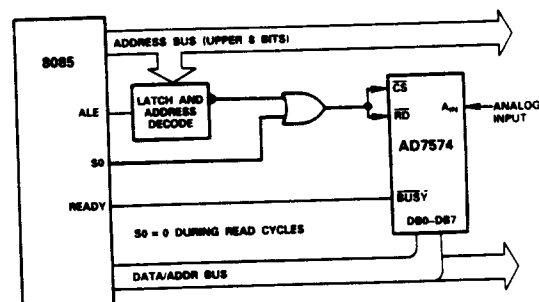


Figure 11. AD7574 to 8085 Slow Memory Mode Interface

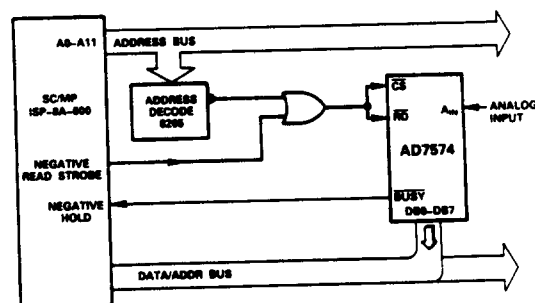


Figure 12. AD7574 to SC/MP Slow Memory Mode Interface

RANGE SWITCHING APPLICATIONS

By means of suitable switching on the AD7574 B_{OFF} and V_{REF} pins, the AD7574 can be made to operate with a range of different attenuation or gain factors. The B_{OFF} or bipolar offset input (pin 3) is used to modify the effective analog input voltage and is normally used to obtain bipolar operation. Figure 13 shows a simple, 3 range, switching arrangement for a 0-20V analog input signal. The full scale input ranges and LSB weights are given in Table I.

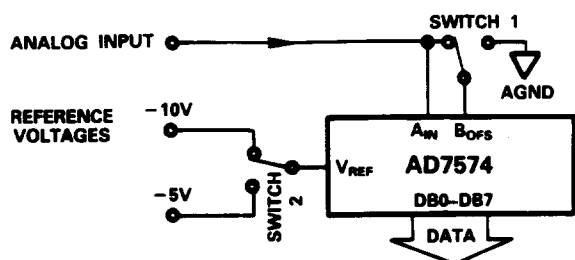


Figure 13. Range Switching the AD7574

BOFS	V _{REF}	Full Scale Input Range	LSB Weight
To A _{IN}	-5V	0V to +5V	19mV
To A _{IN}	-10V	0V to +10V	39mV
To GND	-10V	0V to +20V	78mV
To GND	-5V	0V to +10V	39mV

Table I. AD7574 Input Ranges

The range switching can easily be controlled by the processor using analog switches such as the AD7592 which contains 2 independent SPDT CMOS switches with data latches specifically designed for microprocessor interface.

Figure 14 shows a typical range switching applications circuit with the AD7574 operating in the the slow-memory mode. Since bus conflicts have been eliminated, a WRITE to the AD7574 address selects the analog input voltage range (see Table II) and a READ from the AD7574 address initiates a conversion and reads data when the conversion is complete.

The range selection code is latched by the AD7592 and so need only be considered when a change in analog input range is required.

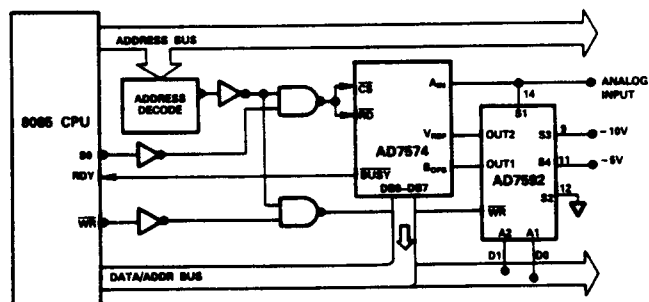


Figure 14. AD7574/8085 Interface with Range Switching

D1	D0	Analog Input Range
0	0	0V to +10V
0	1	0V to +5V
1	0	0V to +20V
1	1	0V to +10V

Table II. Analog Input Range vs. Digital Code to AD7592 for Figure 14

Note: If it is required to use this approach in a system where the WRITE operation bus conflict cannot be eliminated due to timing difficulties, then by decoding a separate address for the AD7574 and the AD7592 the need for a WRITE operation to the AD7574 address can be avoided.

INPUT MULTIPLEXING APPLICATIONS

This application uses the same principles as the range switching application. The analog switching devices have been changed to AD7590s to reduce the package count. The AD7590 consists of four independent SPST CMOS analog switches with on chip data latches (see Figure 15).

Using two AD7590 devices and connecting the data bus directly to the AD7590 control inputs, 8 analog input channels can be multiplexed. The software design must ensure that only one channel is selected at a time. Errors introduced by the analog switch resistance are not significant but can be eliminated by buffering the AD7574 B_OFS and A_IN inputs.

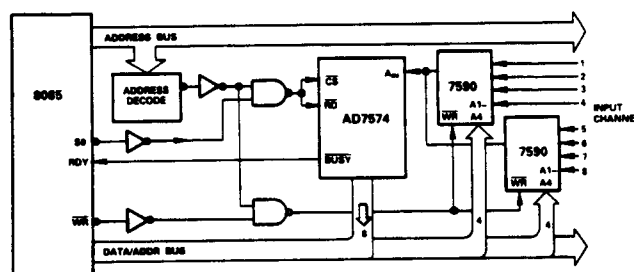


Figure 15. AD7574/8085 Interface with Input Multiplexing of 8 Analog Inputs

A WRITE to the AD7574 address selects an input channel and latches it. A READ from the AD7574 address initiates a conversion and reads data when the conversion is complete.

INTERNAL CLOCK OPERATION

Figure 16 shows a simplified equivalent circuit for the AD7574 internal clock. It operates only during conversion and reset operations, pulses are generated by the action of C charging through R, and discharging through switch 1.

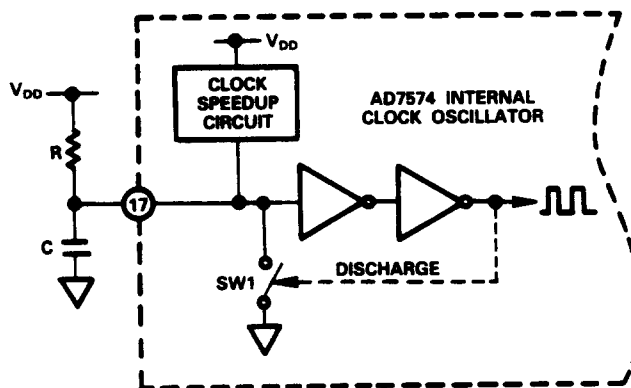


Figure 16. Simplified AD7574 Internal Clock Circuit

A clock speedup circuit shortens the last clock space period in each conversion cycle to reduce overall conversion time. Figure 17 shows a RAM mode timing sequence using the internal clock; other modes have similar timing.

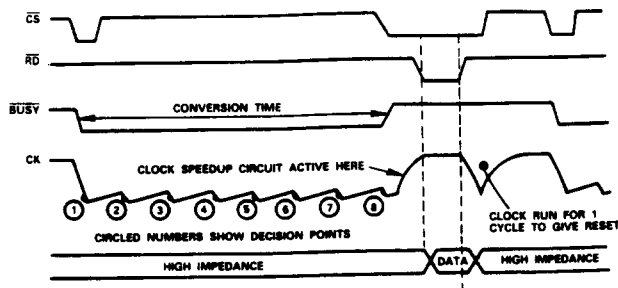


Figure 17. RAM Mode Timing Sequence

Typical values for internal clock timing components can be determined from the graph in the AD7574 data sheet (Figure 7a).

EXTERNAL CLOCK INFORMATION

To obtain dynamic conversion accuracy to rated specification the clock frequency must not exceed 500kHz. The user should understand that normal lot to lot variations in MOS transistor characteristics will cause lot to lot differences in the internal clock oscillator frequency for a given clock R and C.

Additionally, temperature dependence of these MOS characteristics results in thermal drift of internal clock frequency. For this reason, Analog Devices recommends using an external clock in the following situations:

1. Applications having clock frequency within 10% of the 500kHz maximum.
2. Applications where software constraints on time cannot accommodate conversion time differences which

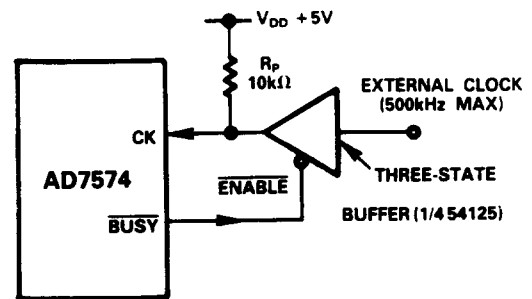


Figure 18. External Clock Connection

may occur due to temperature drift of the internal clock.

Conflicts between the external clock and the internal speedup and reset operations can be avoided by connecting the external clock using the arrangement shown in Figure 18. The three-state buffer is only enabled when the $\overline{\text{BUSY}}$ output is LOW. This ensures that the AD7574 uses the external clock only during the A/D conversion period, i.e., while $\overline{\text{BUSY}}$ is LOW. Internal clock operation is then used with R_p and internal capacitance to give the single clock pulse required for the internal reset.

Since the internal logic of the AD7574 is triggered on falling clock edges, conversion time is reduced if the clock input is at a HIGH level before a conversion starts. This is accomplished by using resistor R_p to pull up the device clock input after the internal reset operation. R_p can be in the range 6kΩ to 100kΩ and simply provides a charge path for the CLK pin capacitance.